Abstract of the Disclosure

A method of forming an interconnection line in a semiconductor device is provided. A first etching stopper is formed on a lower conductive layer which is formed on a semiconductor substrate. A first interlayer insulating layer is formed on the first etching stopper. A second etching stopper is formed on the first interlayer insulating layer. A second interlayer insulating layer is formed on the second etching stopper. The second interlayer insulating layer, the second etching stopper, and the first interlayer insulating layer are sequentially etched using the first etching stopper as an etching stopping point to form a via hole aligned with the lower conductive layer. A protective layer is formed to protect a portion of the first etching stopper exposed at the bottom of the via hole. A portion of the second interlayer insulating layer adjacent to the via hole is etched using the second etching stopper as an etching stopping point to form a trench connected to the via hole. The protective layer is removed. The portion of the first etching stopper positioned at the bottom of the via hole is removed. An upper conductive layer that fills the via hole and the trench and is electrically connected to the lower conductive layer is formed.

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